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Claims

[c1] 1. A color management structure for a panel display, comprising:
a display array unit;
a plurality of gate drivers;
a plurality of source drivers, said plurality of gate drivers and said plurality of source drivers driving said display array unit to display an image; and
a timing sequence control unit, said timing sequence control unit outputting a plurality of signals to said plurality of gate drivers and said plurality of source drivers to drive said display array unit, said timing sequence control unit outputting a clock signal and a color management data to said plurality of source drivers.

[c2] 2.The color management structure of claim 1, wherein said color management data is adjustable.

[c3] 3.The color management structure of claim 1, wherein said panel display is a liquid crystal display.

[c4] 4. The color management structure of claim 1, wherein said timing sequence control unit includes:
a timing controller receiving a system input and provid-

ing said clock signal; and

a color management control block, coupled to said timing controller, outputting said color management data and said clock signal to said plurality of source drivers, said color management data being adjustable.

[c5] 5. The color management structure of claim 4, wherein said color management control block includes:

a storing unit storing a color management basic data; and

a processing unit receiving said color management basic data and an output of said timing controller and outputting said color management data and said clock signal.

[c6] 6.The color management structure of claim 1, wherein each of said plurality of source drivers includes:

a source drive circuit to driving said display array unit; and

a programmable data interface receiving said color management data and said clock signal to parallel output a plurality of color voltage level signals to said source drive circuit.

[c7] 7.The color management structure of claim 6, wherein said plurality of color voltage level signals includes a plurality of color gamma voltage level data.

[c8] 8.The color management structure of claim 6, wherein said programmable data interface includes:
an input interface receiving said color management data and said clock signal and translating said color management data via a data format;
a decoder receiving said translated color management data and said clock signal and decoding said translated color management data, and outputting a decoded data and a control signal; and
a digital-to-analog converting unit receiving said decoded data, said control signal, and said clock signal, and parallel outputting said plurality of color voltage level signals.

[c9] 9. The color management structure of claim 8, wherein said input interface converts a serial input signal into a plurality of parallel output signals based on said clock signal.

[c10] 10. The color management structure of claim 8, wherein said digital-to-analog converting unit includes:
a shift register receiving an output of said decoder;
a latch receiving an output of said shift register and receiving said output of said decoder; and
a plurality of digital-to-analog converters, coupled to said latch, corresponding to said plurality of color volt-

age level signals respectively.

[c11] 11.The color management structure of claim 1, wherein said timing sequence control unit is integrated into an application specified integrated circuit (ASIC).

[c12] 12.A source driver for driving a display array unit of a panel display, said source driver comprising:
a source drive circuit to driving said display array unit; and
a programmable data interface receiving a color management data and a clock signal to parallel output a plurality of color voltage level signals to said source drive circuit.

[c13] 13.The source driver of claim 12, wherein said plurality of color voltage level signals includes a plurality of color gamma voltage level data.

[c14] 14.The source driver of claim 12, wherein said programmable data interface includes:
an input interface receiving said color management data and said clock signal and translating said color management data via a data format;
a decoder receiving said translated color management data and said clock signal and decoding said translated color management data, and outputting a decoded data

and a control signal; and
a digital-to-analog converting unit receiving said decoded data, said control signal, and said clock signal, and parallel outputting said plurality of color voltage level signals.

[c15] 15. The source driver of claim 14, wherein said input interface converts a serial input signal into a plurality of parallel output signals based on said clock signal.

[c16] 16. The source driver of claim 14, wherein said digital-to-analog converting unit includes:
a shift register receiving an output of said decoder;
a latch receiving an output of said shift register and receiving said output of said decoder; and
a plurality of digital-to-analog converters, coupled to said latch, corresponding to said plurality of color voltage level signals respectively.

[c17] 17. A color management structure for a panel display, comprising:
a display array unit;
a plurality of gate drivers;
a plurality of source drivers, said plurality of gate drivers and said plurality of source drivers driving said display array unit to display an image;
a timing sequence control unit, said timing sequence

control unit outputting a plurality of signals to said plurality of gate drivers and said plurality of source drivers to drive said display array unit, said timing sequence control unit outputting a clock signal; and
a color management interface system, coupled to said timing sequence control unit and said plurality of source drivers, generating a color management data to said plurality of source drivers.

[c18] 18.The color management structure of claim 17, wherein said color management interface system includes a color management control block in said timing sequence control unit and a color data converting unit in each of said plurality of source drivers to obtain a plurality of color voltage level signals for said plurality of source drivers.

[c19] 19.A panel display comprising:
a display array unit;
a plurality of drivers driving said display array unit to display an image; and
a timing sequence control unit, said timing sequence control unit outputting a plurality of signals to said plurality of drivers to drive said display array unit, said timing sequence control unit outputting a clock signal and a color management data to said plurality of drivers.

[c20] 20. The panel display of claim 19, wherein said color

management data is a serial color management correction data.

[c21] 21. A color management method for a panel display, said panel display including a display array unit, a plurality of drivers, and a timing sequence control unit, said timing sequence control unit outputting a plurality of signals to said plurality of drivers to drive said display array unit, said color management method comprising:
generating a serial color management data via said timing sequence control unit, according to a clock signal;
converting said serial color management data to a plurality of parallel analog color data signals; and
inputting said plurality of parallel analog color data signals to said plurality of drivers to correct a color of a pixel.